

Advanced course on Embedded Systems design using FPGA

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Abstract-As the number of embedded system applications and their complexities are increasing there is a demand to use the advanced technologies for embedded system design. This course describes the concepts of system design with the latest FPGAs (Field programmable gate arrays) which can also implement soft-core microcontrollers, and lists a number of laboratory exercises and end of the semester course projects. This course covers the design of advanced FPGAs with soft-core micros and interface to hard-core micros and applications.

The applications taught include digital signal processing, image processing, display, automotive navigation etc. This paper describes a senior undergraduate/ graduate level course with details of the topics taught, text books to use, software tools to use, the lab exercises and suitable projects.

Index- Embedded System, FPGA, FPGA Design

INTRODUCTION

Embedded systems need increase in performance and more functions often. There is a need for integration of more devices and chips, decrease in power consumption, cost, size and time to market. Price of complex FPGAs with 32 bit soft microprocessor core are falling and are closer to the microprocessor system price. Altera and, Xilinx are leading FPGA chip manufacturers, and they have a number of devices for embedded system market at different price ranges. FPGA represents the logical extension in the “hard to soft” migration of system functionality. Software tools for FPGA are growing and becoming easier. Processors, peripheral devices, logic, and software can be changed in FPGA system even after manufacturing, leading to easier re-configurability and upgradability. Hence this course is a valuable course for senior undergraduate and graduate students interested in embedded systems.

TOPICS COVERED

This is a Hardware and software design and project oriented course. The text book used is by Zainalabedin Navabi [1]. And the topics covered are:

- Elements of Embedded Systems Design
- Real Time systems Requirements
- Field Programmable devices
- VHDL based design and design of Logic modules
- Simple CPU design
- Tools for design and Prototyping
- Device Drivers for FPGA cores
- Design with embedded processors
- Design of FPGA based embedded systems and interface to hard-core micros
- Low Power FPGA based Systems
- Automotive applications

COURSE OBJECTIVE:

Upon successful completion of the course students will be able to design FPGA based embedded systems with soft-core microcontrollers and develop software. Students also learn to work in a team environment and communicate the results as written reports and oral presentations.

SOFT-CORE MICRO TOPICS:

NIOS is a configurable Soft-Core 32 bit processor, based on general purpose RISC processor core similar to MIPS. It has flexible peripheral set, address map and custom instructions. It can be implemented inside many Altera FPGA chips, including Cyclone II. This is implemented by software on the FPGA chips. One can also implement multiple NIOS processors inside the FPGA chip. Similarly a soft core processor can be implemented in the Xilinx Spartan 3E and others. We describe the design of the CPU, selection of instruction and implementation of NIOS. Students implement them in the lab and write programs to test and use them. They also learn how to interface a FPGA to a external microprocessor. This is needed since many

complex applications require multiprocessing with FPGA and microprocessor.

LABORATORY EXERCISES

Altera sells DE2 boards (Figure 1) which are ideal for class room purpose. The board contains the Cyclone II 2C35 FPGA, toggle switches, push button switches, LEDs and 7 segment displays. One can also interface, SRAM, SDRAM, Flash memory chips, 16x2 character displays, RS-232 and PS/2, connectors for microphone, line-in, line-out, video-in, VGA, USB, Ethernet, infrared port and expansion headers. This board comes with Quartus II software development system.

Lab assignments using FPGA development boards (DE2 Altera boards with cyclone 2 FPGAs and Quartus II software development tools and Xilinx Spartan 3) with emphasis on **design** are given.

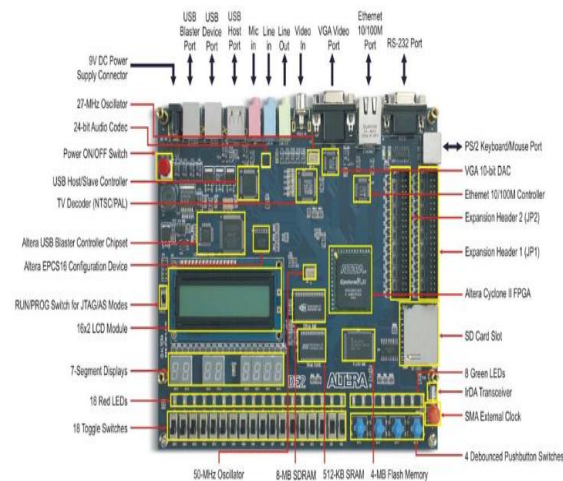


FIGURE 1
DE2 ALTERA BOARD

Lab1: Switches, LED Lights and Mux using VHDL programming

Lab 2: Use of Library module for Full adder design with 7 seg display

Lab3: FlipFlop, Registers for a complex circuit design

Lab 4: Integrate a CCD camera and LCD panel display

Lab 5: NIOS 2 processor implementation.

For each lab, the students submit **objective, a flow chart, hardware interface details, and opcode** with comments.

PROJECT

Students do a small group project, demonstrate the project, make a presentation in the class and also submit a report. A short list of projects done during the second half of the semester are the following.

Solar Tracking, Interfacing the LCD and Camera, Edge detection, TV box application (Figure 2) and Karaoke audio system (Figure 3) Some of the projects are described briefly.

I. TV BOX APPLICATION

Figure 2 shows a Video application where the information may come from a DVD player or a video camera. Students write applications and algorithms to display the image on the VGA monitor and process the image with video processing algorithms. Some algorithms are tested using Matlab tools and then ported to this board manually re-writing the C code.

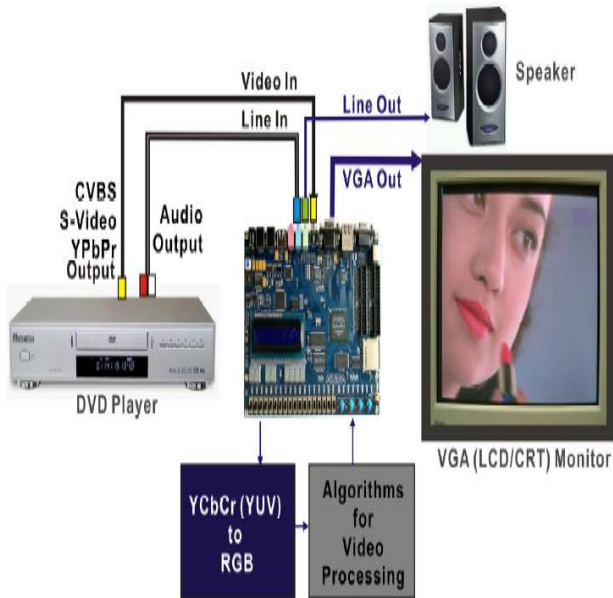


FIGURE 2
TV BOX APPLICATION

II. KARAOKE APPLICATION

Figure 3 shows the setup for a simple audio application. Students write programs to mix audio signals and play it on the audio output. The algorithms are tested using Matlab tools and then ported to this board with the required modifications. This demonstration uses the microphone-in, line-in, and line-out ports on the DE2 board to create a Karaoke Machine application. The Wolfson WM8731 audio CODEC is configured in the master mode, where the audio CODEC generates AD/DA serial bit clock (BCK) and the left/right channel clock (LRCK) automatically. As indicated in Figure 3, the I2C interface is used to configure the Audio CODEC. The sample rate and gain of the CODEC are set in this manner, and the data input from the line-in port is then mixed with the microphone-in port and the result is sent to the line-out port. For this demonstration the sample rate is set to 48 kHz. Pressing the pushbutton *KEY0* reconfigures the gain of the audio CODEC via the I2C bus, cycling through one of the ten predefined gains (volume levels) provided by the device.

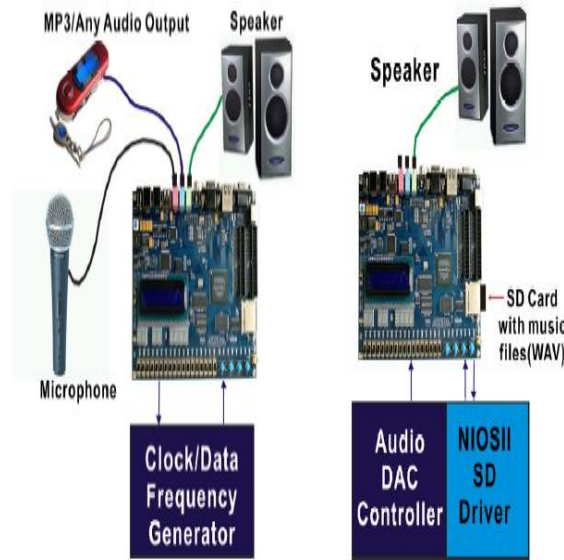


FIGURE 3
KARAOKE MACHINE

III. SPEAKER RECOGNITION

The goal for our project was to be able to distinguish, in real time, between various speakers based only on audio input. In the literature, this problem is known as speaker recognition, or, more precisely, speaker identification. A good deal of progress has been made in this field, but it is still an open research topic, and by no means a solved problem. Speaker recognition is applicable to many fields, including but not limited to artificial intelligence, cryptography, and national security [2].

IV. IMAGE MANIPULATION USING DE2 FPGA

DEVELOPMENT BOARD, 5 MEGAPIXEL CAMERA CARD, AND TOUCH SCREEN DISPLAY

This project goal is to demonstrate the use of the Cyclone II FPGA chip to provide an interface between a TRDB_D5M digital camera development kit (input signal) and a TRDB_LTM 4.3 Inch Digital Touch Panel development kit (output signal destination) (shown in Figure 4). The system will receive real time video data from the CCD lens and will convert the raw image data into a format that can be displayed on the LTM screen. In addition to the simple collection and output of the image data, the FPGA will be used to perform image manipulation in the form of grayscale and monochrome conversion of the captured video data stream. This type of manipulation is a common initial step used when performing functions such as edge

detection and object classification algorithms. The choice of which type of output is displayed will be determined by the user interaction with the touch screen device. The user will tap the screen to signal to the system that a change in the output type is required. The details of the implementation of the project as well as the challenges and opportunities for future development are part of the student project report. The system/ major function blocks are shown in the Figure 5.

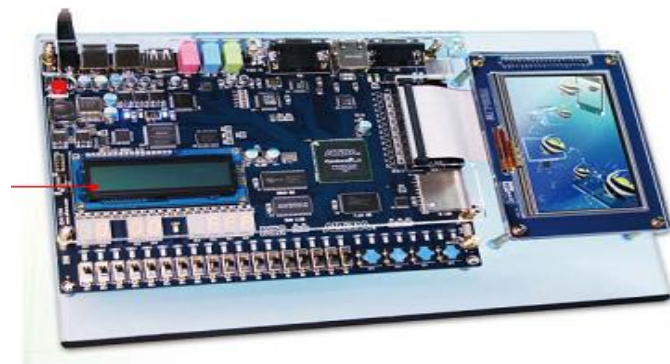


FIGURE 4
CAMERA INTERFACE AND TOUCH PANEL LCD INTERFACE.

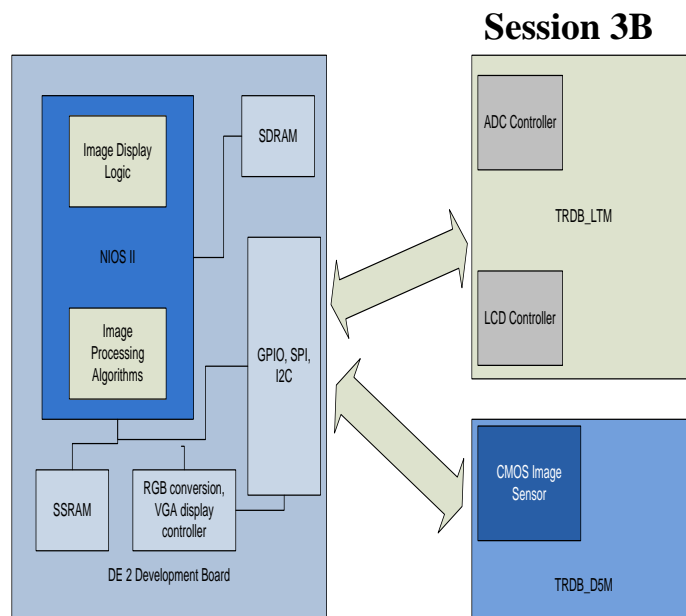


FIGURE 5
SYSTEM LEVEL BLOCK DIAGRAM

CLASS PRESENTATIONS

Students make a 15 minute presentation in the class. This is individual presentation and is different from the project team's group presentation. A sample list of topics presented is:

- Xilinx latest FPGA (Virtex 5 or 6) and applications--
- Altera – Latest FPGA (Stratix 3) and applications--
- Lattice FPGA and applications---
- eASIC nextreme cells, www.easic.com -
- Actel IGLOO FPGAs --
- MathStar Field Programmable object array; www.mathstar.com --
- Reconfigurable computing with FPGAs-
- Signal Processing in (with) FPGAs --
- How FPGAs enable automotive system s—
- Altera.com paper —
- Implement security in Spartan FPGAs --
- Profiling NIOS II; www.altera.com/literature/an/an391.pdf --
- FPGA in automotive Radars -
- www.smartmicro.de/using_FPGAs_in_Automotive_radar_sensors_V7.pdf
- FPGA code generation using Matlab
- Open source and freeware FPGA tools

- www.jhdl.org;
 - www.opencores.org;
 - www.ghdl.free.fr;
 - www.myhdl.org
- Solar Tracking control using FPGA ---
- www.altera.com/literature/dc/2007/t3c.pdf;
www.pld-design.com
- LogicCraft3 FPGA based multimedia development,
 - www.logibricks.com;
 - Xilinx.com
- FPGA considerations for automotive applications—SAE paper
- Leveraging FPGA coprocessors to optimize automotive infotainment Altera paper
- A dual priority real time multiprocessor system on FPGA
- Advantage of FPGA based multiprocessor system in Industrial Applications—

CONCLUSION

This paper describes a course on advanced embedded systems design using FPGA and covers the design of advanced FPGAs with soft-core micros and interface to hard-core micros and applications. A list of projects done and presentation topics are also given. As the technology changes fast, each year this course will be taught with new FPGA chips and boards.

REFERENCES

- [1] Sainlabedin Navabi “Embedded core design with FPGAs” McGraw Hill, 2007, ISBN-978-0-07-147481-8
- [2] http://courses.cit.cornell.edu/ece576/FinalProjects/f2008/pae26_jsc59/pae26_jsc59/index.html for speaker recognition project.